

FREQUENCY LOCKED LOOP

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ABSTRACT OF THE DISCLOSURE

A frequency locked loop in a microcontroller integrated circuit has a precision digital feedback control loop. The frequency locked loop performs a clock multiplication function such that an inexpensive and low frequency external crystal is usable to both clock a processor of the microcontroller with a higher frequency and low-jitter clock signal and to clock a real time clock of the microcontroller with a low frequency time base that is a power of two multiple of one hertz. In one embodiment, the digital feedback control loop includes a ramp generator, a digital filter, and a loop divider. The ramp generator is controlled to output steeper and steeper ramps as the frequency locking process proceeds toward frequency lock. A preset value that presets the loop divider is changed to adjust the phase of a feedback signal with respect to a reference input signal.